AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

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a first circuit configured to ~~(i)~~ change a frequency of one or more ~~first~~ clock signals in response to ~~a second signal and~~ ~~(ii)~~ one or more first control signals;

a second circuit configured to generate said one or more first control signals and a ~~third~~ second control signal; and

a third circuit configured to generate a first reset signal in response to either said second control signal or a predetermined time period expiring.

2. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said ~~second signal programs~~ one or more first control signals are configured to program said frequency of said one or more clock signals.

3. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said one or more ~~first~~ clock signals are generated by one or more phase lock loop circuits.

4. (CURRENTLY AMENDED) The apparatus according to claim 3, wherein said ~~second signal programs~~ one or more first control

signals are configured to program at least one of said one or more phase lock loop circuits.

5. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said one or more ~~first~~ clock signals are generated using a divider network.

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6. (ORIGINAL) The apparatus according to claim 1, wherein said predetermined time period is programmable.

7. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said second circuit is further configured to generate a third control signal and said predetermined time period is started in response to said ~~second~~ third control signal.

8. (CURRENTLY AMENDED) The apparatus according to claim ~~1~~ 7, wherein said third circuit further comprises a watchdog timer circuit ~~that measures~~ configured to measure said predetermined time period in response to said third control signal.

9. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein one of said ~~first~~ one or more clock signals is presented to a clock input of a processor and said ~~third~~ first reset signal is presented to a reset input of said processor.

10. (CURRENTLY AMENDED) The apparatus according to claim 9, wherein said ~~second signal is~~ one or more first control signals are generated using a number of instructions executed by said processor.

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11. (ORIGINAL) The apparatus according to claim 10, wherein said instructions are contained in a computer readable medium.

12. (ORIGINAL) The apparatus according to claim 10, wherein said instructions are part of a basic input output system (BIOS) routine.

13. (ORIGINAL) The apparatus according to claim 9, wherein said predetermined time period expires only when said processor hangs.

14. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said third circuit is further configured to generate a ~~fourth~~ a second reset signal in response to the expiration of said predetermined time period.

15. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said second circuit comprises an inter-integrated circuit (I^2C) interface circuit.

16. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein:

said first circuit ~~is~~ further comprises a logic circuit configured to control a skew of each of said one or more first signals in response to a third control signal; and

said second circuit is configured to generate said third control signal.

17. (ORIGINAL) The apparatus according to claim 16, wherein said skew is programmable.

18. (CURRENTLY AMENDED) An apparatus comprising:

means for changing a frequency of one or more ~~first~~ clock signals in response to ~~a second signal~~ one or more first control signals;

means for generating said one or more first control signals and second control signal; and

means for generating a ~~third~~ reset signal in response to either said second control signal or a predetermined time period expiring.

19. (CURRENTLY AMENDED) A method for recovering in a phase lock loop circuit from a processor hang due to over-clocking comprising the steps of:

(A) changing a frequency of a clock signal in response to one or more first control signals;

(B) ~~resetting~~ generating said one or more first control signals and a second control signal, wherein said processor is reset in response to said second control signal when said frequency ~~change~~ is changed; and

(C) detecting whether said processor hangs in response to said frequency change.

20. (ORIGINAL) The method according to claim 19, further comprising the step of:

(D) when said processor hangs, changing said frequency of said clock signal to a fail-safe frequency and resetting said processor.

21. (CURRENTLY AMENDED) The apparatus according to claim 14, wherein:

said ~~third~~ first reset signal is configured to reset a processor; and

said ~~fourth~~ second reset signal is configured to reset an entire system.